

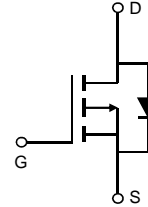
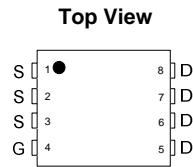
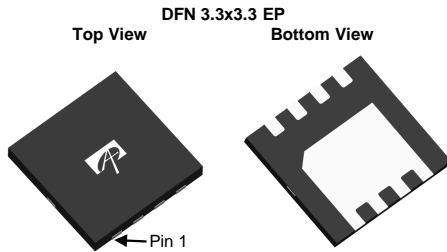
### General Description

The GXN7423 combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

### Product Summary

$V_{DS}$	-20V
$I_D$ (at $V_{GS}=-4.5V$ )	-50A
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$ )	< 5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-2.5V$ )	< 6.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-1.8V$ )	< 8.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-1.5V$ )	< 11m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	-50
		$T_C=100^\circ\text{C}$	-39
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-200	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	-28
		$T_A=70^\circ\text{C}$	-22.5
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	60	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	180	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	83
		$T_C=100^\circ\text{C}$	33
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	6.2
		$T_A=70^\circ\text{C}$	4
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16	20	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient <sup>A,D</sup>				
Maximum Junction-to-Case	$R_{\theta JC}$	1.1	1.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-20\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 8\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-0.2	-0.5	-0.9	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}, V_{DS}=-5\text{V}$	-200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5\text{V}, I_D=-20\text{A}$ $T_J=125^\circ\text{C}$		3.95	5	m $\Omega$
				5.7	7.2	
		$V_{GS}=-2.5\text{V}, I_D=-20\text{A}$		4.9	6.5	m $\Omega$
		$V_{GS}=-1.8\text{V}, I_D=-20\text{A}$		6.1	8.5	m $\Omega$
	$V_{GS}=-1.5\text{V}, I_D=-20\text{A}$		7.7	11	m $\Omega$	
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-20\text{A}$		110		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.5	-1	V
$I_S$	Maximum Body-Diode Continuous Current <sup>G</sup>				-50	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-10\text{V}, f=1\text{MHz}$		5626		pF
$C_{oss}$	Output Capacitance			928		pF
$C_{riss}$	Reverse Transfer Capacitance			716		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		3	6	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{GS}=-4.5\text{V}, V_{DS}=-10\text{V}, I_D=-20\text{A}$		70	100	nC
$Q_{gs}$	Gate Source Charge			9.2		nC
$Q_{gd}$	Gate Drain Charge			18.4		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-4.5\text{V}, V_{DS}=-10\text{V}, R_L=0.5\Omega,$ $R_{GEN}=3\Omega$		18		ns
$t_r$	Turn-On Rise Time			52		ns
$t_{D(off)}$	Turn-Off DelayTime			285		ns
$t_f$	Turn-Off Fall Time			123		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-20\text{A}, dI/dt=500\text{A}/\mu\text{s}$		78		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}, dI/dt=500\text{A}/\mu\text{s}$		495		nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA} t \leq 10\text{s}$  value and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

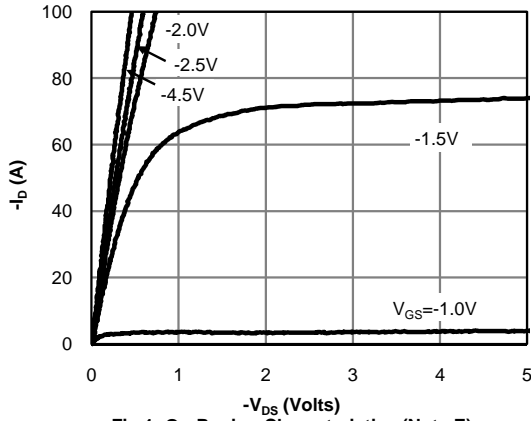
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

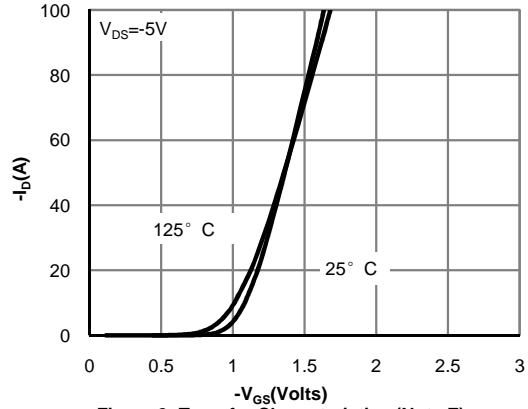
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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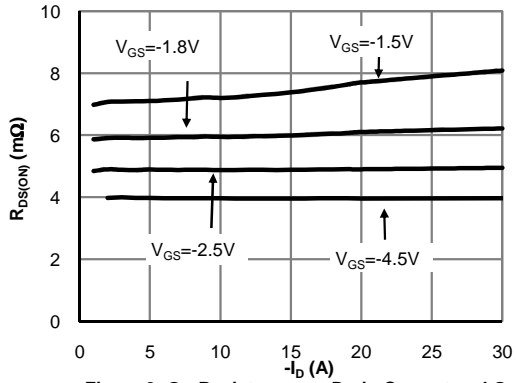
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



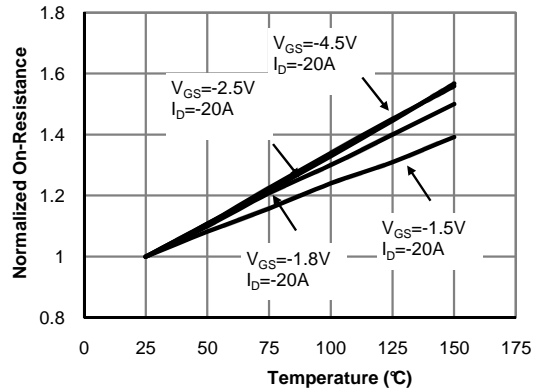
**Fig 1: On-Region Characteristics (Note E)**



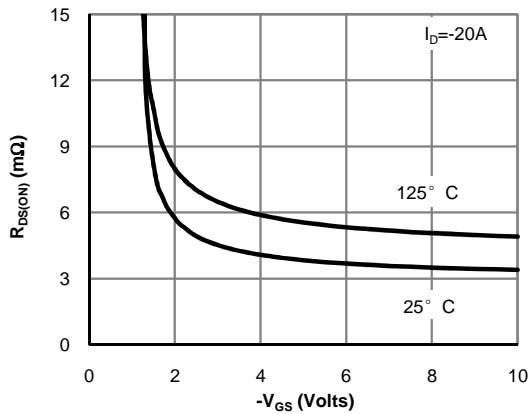
**Figure 2: Transfer Characteristics (Note E)**



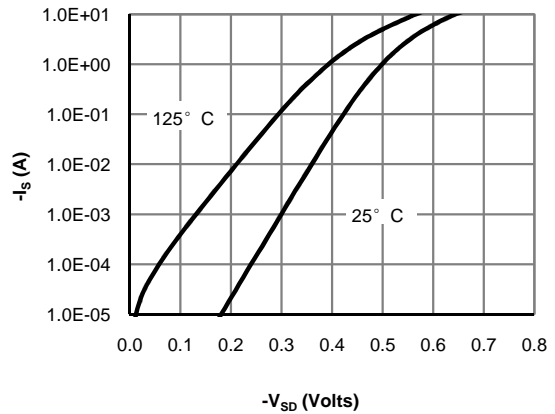
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

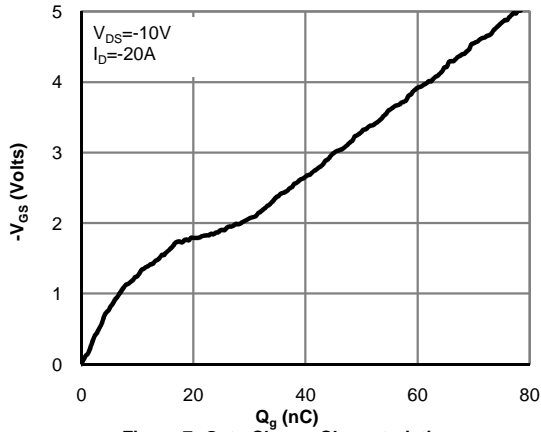


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

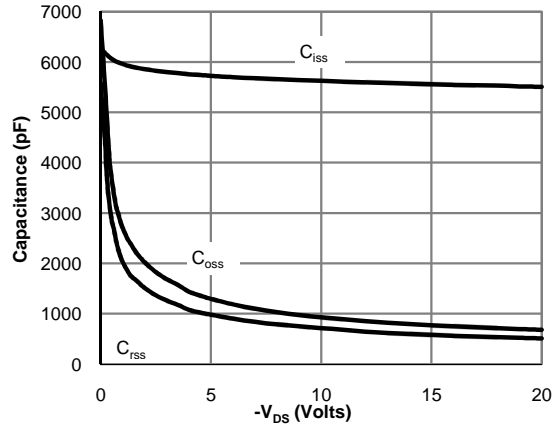


**Figure 6: Body-Diode Characteristics (Note E)**

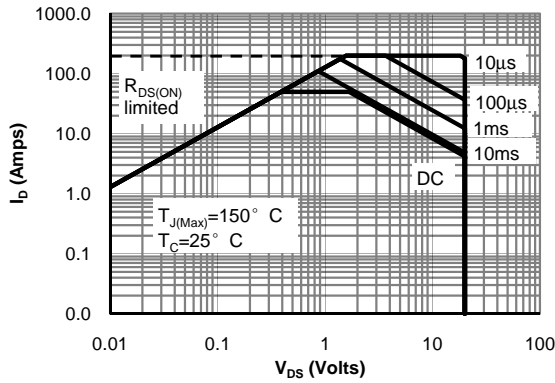
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



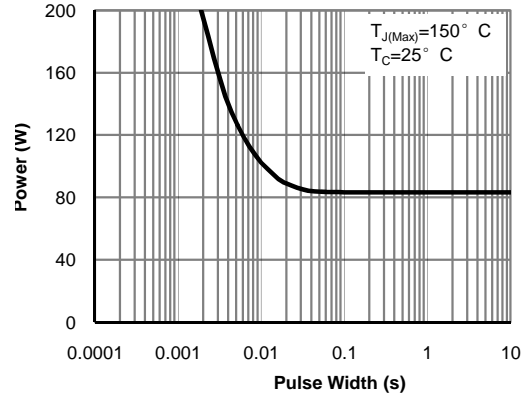
**Figure 7: Gate-Charge Characteristics**



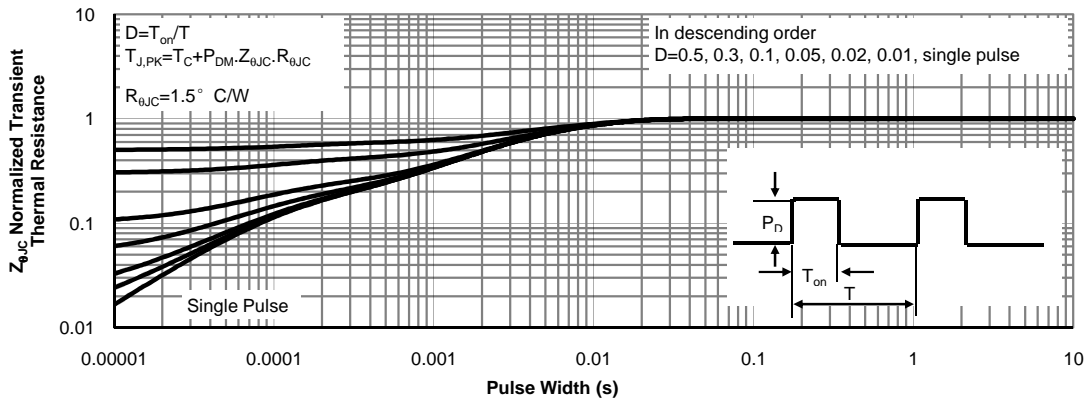
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

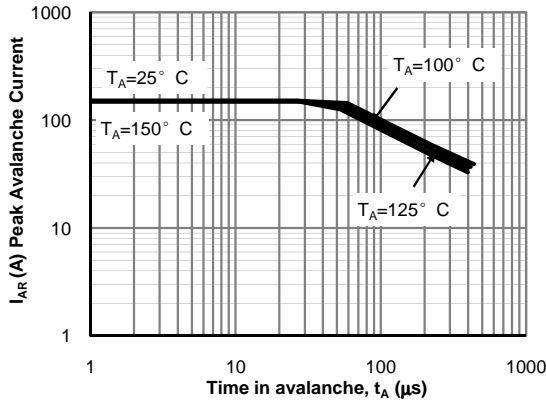


**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

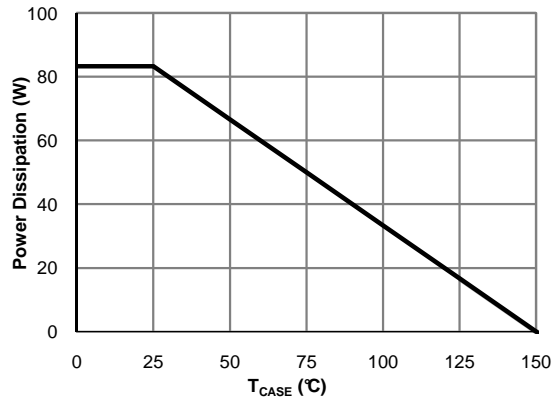


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

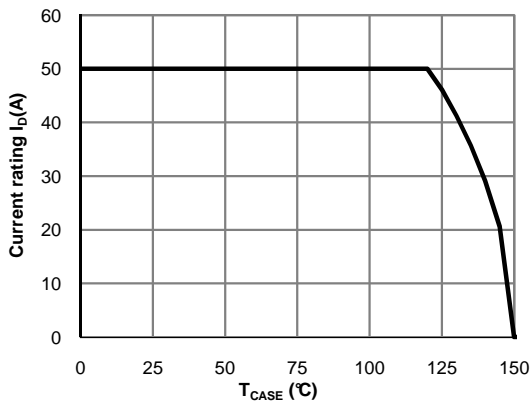
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



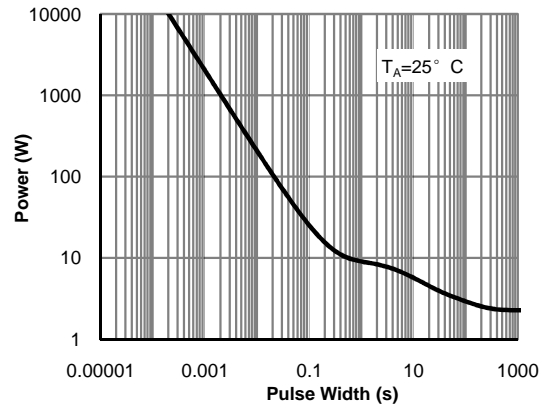
**Figure 12: Single Pulse Avalanche capability (Note C)**



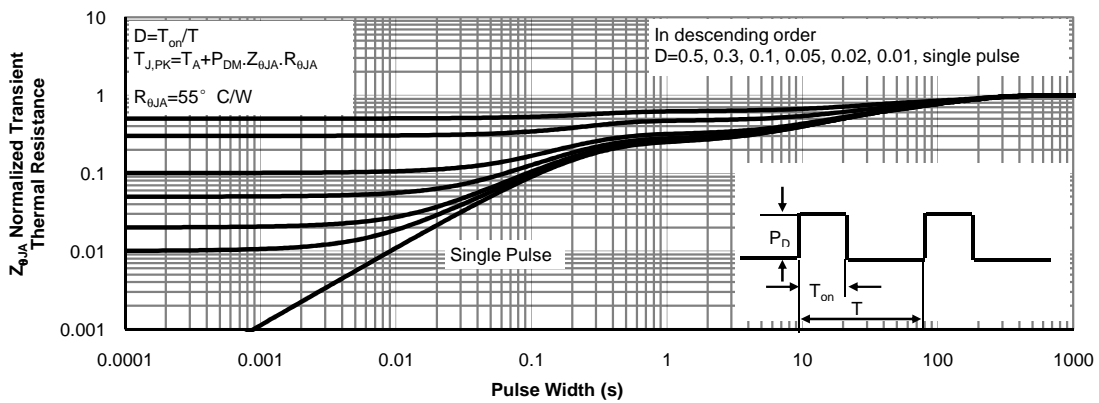
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

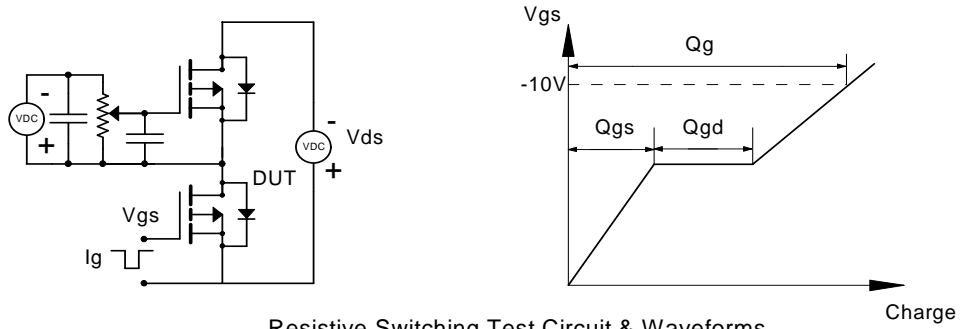


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

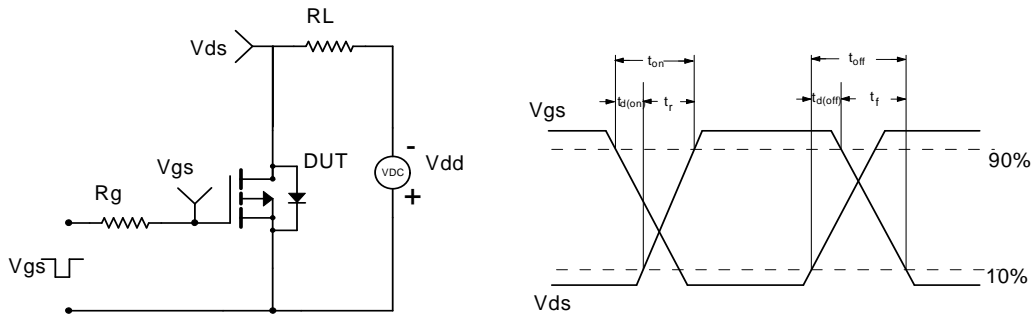


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

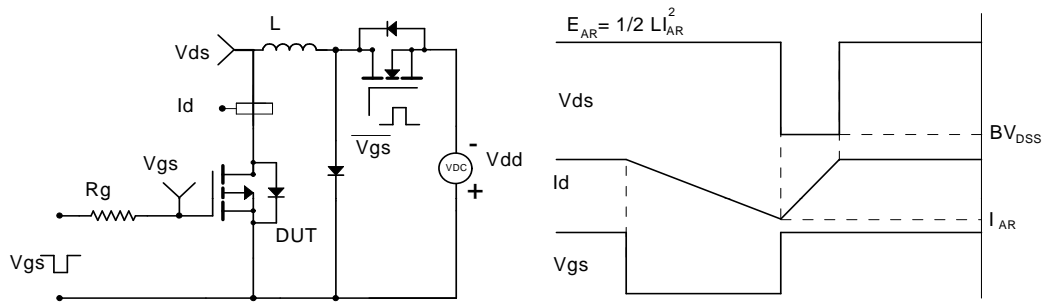
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

